Pending Claims:

This listing of claims is provided below. No amendment to the claims has been made.

Listing of Claims:

1-10. (Canceled)

11. (Previously presented) A delay locked loop (DLL) for compensating for a skew between an external clock signal and an output data signal in a memory device, comprising:

a digital locking circuit configured to receive the external clock signal and generate a DLL clock signal, wherein the DLL clock signal is a delayed version of the external clock signal; and

an analog locking circuit configured to receive the DLL clock signal from the digital locking circuit and check a delayed version of the DLL clock signal against the external clock signal to generate a feedback signal that is fed back to the digital locking circuit.

12. (Previously presented) The delay locked loop according to claim 11 wherein the feedback signal is used by the digital locking circuit to adjust the DLL clock signal.

13. (Previously presented) The delay locked loop according to claim 11 wherein the analog locking circuit checks the delayed version of the DLL clock signal against the external clock signal by detecting a phase difference between the delayed version of the DLL clock signal and the external clock signal; and

wherein the detected phase difference is used by the analog locking circuit to generate the feedback signal so as to cause the digital locking circuit to adjust the DLL clock signal accordingly.

14. (Previously presented) The delay locked loop according to claim 13 wherein the DLL clock signal is generated by delaying the external clock signal by a predetermined time interval, wherein the predetermined time interval is calculated by subtracting the skew from a time period of the external clock signal; and

wherein the delayed version of the DLL clock signal is generated by delaying the DLL clock signal by the skew.

15. (Previously presented) The delay locked loop according to claim 11 wherein the DLL clock signal is used by the memory device to signal for output data thereby allowing the output data signal to be synchronized with the external clock signal.

16. (Previously presented) The delay locked loop according to claim 11 wherein the digital locking circuit further comprises:

a first delay circuit configured to delay the external clock signal by the skew to generate a delayed clock signal;

a control circuit configured to receive the delayed clock signal and the external clock signal and generate a first pair and a second pair of control signals;

a first voltage controlled oscillation circuit configured to receive the first pair of control signals and generate a measurement oscillating signal;

a second voltage controlled oscillation circuit configured to receive the second pair of control signals and generate a replication oscillating signal; and

a circuit configured to receive the measurement oscillating signal and the replication oscillating signal and generate the DLL clock signal.

17. (Previously presented) The delay locked loop according to claim 16 wherein the first of the first pair of control signals is enabled to a high level from a first rising edge to a second rising edge of the external clock signal, and the second of the

first pair of control signals is enabled to a low level from a first rising edge to a second rising edge of the delayed clock signal.

18. (Previously presented) The delay locked loop according to claim 17 wherein the measurement oscillating signal is toggled while the first pair of control signals are enabled.

19. (Previously presented) The delay locked loop according to claim 16 wherein the analog locking circuit further comprises:

a second delay circuit configured to delay the DLL clock signal by skew to generate a comparison clock signal;

a phase detector configured to detect a phase difference between the comparison clock signal and the external clock signal and generate a phase detector output signal based on the phase difference; and

a voltage control circuit configured to receive the phase detector output signal and generate a voltage control signal that is then fed to the first and second voltage controlled oscillation circuits.

20. (Previously presented) The delay locked loop according to claim 11 wherein the memory device is a synchronous dynamic random access memory.

21. (Previously presented) A computer system incorporating the delay locked loop as recited in claim 11.

22. (Previously presented) A synchronizing circuit for compensating for a skew between an external clock signal and an output data signal in a memory device, comprising:

a digital locking circuit configured to receive the external clock signal and generate an output clock signal, wherein the output clock signal is a delayed version of the external clock signal; and

an analog locking circuit configured to generate a delayed version of the output clock signal received from the digital locking circuit and compare respective phases of the delayed version of the output clock signal and the external clock signal in order to generate a feedback signal that is fed back to the digital locking circuit.

23. (Previously presented) The synchronizing circuit according to claim 22 wherein the feedback signal is used by the digital locking circuit to adjust the output clock signal.

24. (Previously presented) The synchronizing circuit according to claim 22 wherein the output clock signal is generated by delaying the external clock signal by a predetermined time interval, wherein the predetermined time interval is calculated by subtracting the skew from a time period of the external clock signal; and

wherein the delayed version of the output clock signal is generated by delaying the output clock signal by the skew.

25. (Previously presented) The synchronizing circuit according to claim 22 wherein the output clock signal is used by the memory device to signal for output data thereby allowing the output data signal to be synchronized with the external clock signal.

26. (Previously presented) The synchronizing circuit according to claim 22 wherein the digital locking circuit further comprises:

a first delay circuit configured to delay the external clock signal by the skew to generate a delayed clock signal;

a control circuit configured to receive the delayed clock signal and the external clock signal and generate a first pair and a second pair of control signals;

a first voltage controlled oscillation circuit configured to receive the first pair of control signals and generate a measurement oscillating signal;

a second voltage controlled oscillation circuit configured to receive the second pair of control signals and generate a replication oscillating signal; and

a circuit configured to receive the measurement oscillating signal and the replication oscillating signal and generate the output clock signal.

27. (Previously presented) The synchronizing circuit according to claim 26 wherein the first of the first pair of control signals is enabled to a high level from a first rising edge to a second rising edge of the external clock signal, and the second of the first pair of control signals is enabled to a low level from a first rising edge to a second rising edge of the delayed clock signal.

28. (Previously presented) The synchronizing circuit according to claim 27 wherein the measurement oscillating signal is toggled while the first pair of control signals are enabled.

29. (Previously presented) The synchronizing circuit according to claim 26 wherein the analog locking circuit further comprises:

a second delay circuit configured to delay the output clock signal by skew to generate a comparison clock signal;

a phase detector configured to detect a phase difference between the comparison clock signal and the external clock signal and generate a phase detector output signal based on the phase difference; and

a voltage control circuit configured to receive the phase detector output signal and generate a voltage control signal that is then fed to the first and second voltage controlled oscillation circuits.

30. (Previously presented) The synchronizing circuit according to claim 22 wherein the memory device is a synchronous dynamic random access memory.

31. (Previously presented) A computer system incorporating the synchronizing circuit as recited in claim 22.

32. (Previously presented) A delay locked loop for compensating for a skew between an external clock signal and an output data signal in a synchronous dynamic access memory device, comprising:

a first delay circuit configured to delay the external clock signal by a time interval equaling the skew to generate a delayed clock signal;

a control circuit configured to receive the delayed clock signal and the external clock signal and generate a first pair and a second pair of control signals;

a first voltage controlled oscillation circuit configured to receive the first pair of control signals and generate a measurement oscillating signal;

a second voltage controlled oscillation circuit configured to receive the second pair of control signals and generate a replication oscillating signal;

a circuit configured to receive the measurement oscillating signal and the replication oscillating signal and generate an output clock signal; and

a comparison circuit configured to generate a comparison clock signal that is derived from a delayed version of the output clock signal and detect a phase difference between the comparison clock signal and the external clock signal generate a phase detector output signal based on the phase difference, wherein the phase detector output signal is used to adjust the first and second voltage controlled oscillation circuits.

33. (Previously presented) The delay locked loop according to claim 32 wherein the first of the first pair of control signals is enabled to a high level from a first rising edge to a second rising edge of the external clock signal, and the second of the first pair of control signals is enabled to a low level from a first rising edge to a second rising edge of the delayed clock signal.

34. (Previously presented) The delay locked loop according to claim 33 wherein the measurement oscillating signal is toggled while the first pair of control signals are enabled.

35. (Previously presented) The delay locked loop according to claim 32 wherein the comparison clock signal is generated by delaying the output clock signal by the skew.

36. (Previously presented) The delay locked loop according to claim 32 wherein the output clock signal is used by the memory device to signal for output data thereby allowing the output data signal to be synchronized with the external clock signal.

37. (Previously presented) A computer system incorporating the synchronizing circuit as recited in claim 32.

38. (Previously presented) A method for compensating for a skew between an external clock signal and an output data signal in a memory device, comprising:

generating an output clock signal by delaying the external clock signal by a predetermined time interval calculated by subtracting the skew from a time period of the external clock signal;

generating a comparison clock signal by delaying the output clock signal by the skew;

comparing a phase difference between the comparison clock signal and the output clock signal to form a feedback signal; and

using the feedback signal to adjust the output clock signal.

39. (Previously presented) The method according to claim 38 further comprising:

using the output clock signal to signal for output data from the memory device thereby allowing the output data signal to be synchronized with the external clock signal.

40. (Previously presented) The method according to claim 38 wherein the generation of the output clock signal further comprises:

generating a delayed clock signal by delaying the external clock signal by the skew;

using the delayed clock signal and the external clock signal to generate a first pair and a second pair of control signals;

inputting the first pair of control signals to a first voltage controlled oscillation circuit to generate a measurement oscillating signal;

inputting the second pair of control signals to a second voltage controlled oscillation circuit to generate a replication oscillating signal; and

using the measurement oscillating signal and the replication oscillating signal to generate the output clock signal.

41. (Previously presented) The method according to claim 40 further comprising:

enabling the first of the first pair of control signals to a high level from a first rising edge to a second rising edge of the external clock signal; and

enabling the second of the first pair of control signals to a low level from a first rising edge to a second rising edge of the delayed clock signal.

42. (Previously presented) The method according to claim 41 further comprising:

toggling the measurement oscillating signal while the first pair of control signals are enabled.